A RADIO ARCHITECTURE FOR USE WITH FREQUENCY DIVISION DUPLEXED SYSTEMS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 60/215,711, entitled "Receiver Architecture for Frequency Domain Duplexed Systems such as WCDMA", having attorney docket No. TI-31261PS, and filed on July 3, 2000.

TECHNICAL FIELD

This invention relates in general to the field of radio communications and more specifically to a radio architecture for use with frequency division duplexed (FDD) systems.

BACKGROUND

Given the huge proliferation of radio communication devices in the last several years with the advent of communication systems like cordless telephones, cellular and personal communication system (PCS) radiotelephones, etc. several possible receiver architectures exist for implementing a radio frequency (RF) receiver. Some of the most prevalent receiver architectures currently in use today are the Superheterodyne receiver,

the direct conversion or Homodyne receiver, and the wide-band IF with double conversion receiver. A discussion of these different receiver architectures can be found in an article found in the IEEE journal of Solid-State Circuits, Vol. 32, No. 12, December 1997, entitled "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications" by Rudell, et al. Each of the receiver architectures mentioned above has its own unique advantages and disadvantages.

The largest interfering source (also referred to as "interferer") in a frequency division duplex (FDD) radio, such as a wide-band code division multiple access (WCDMA) transceiver, is the output signal from the transmitter's power amplifier. The transmitter output signal can interfere with and sometimes degrade the performance of the transceiver's receiver section. A radio architecture that could help minimize the noted interference problem would be beneficial.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the present invention, which are believed to be novel, are set forth with particularity in the appended claims. The invention, may best be understood by reference to the following description, taken in conjunction with the accompanying drawings, in the several figures of which like reference numerals identify like elements, and in which:

FIG. 1 shows a block diagram of radio architecture in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

While the specification concludes with claims defining the features of the invention that are regarded as novel, it is believed that the invention will be better understood from a consideration of the following description in conjunction with the drawing figure.

The receiver architecture of the present invention reduces the effect of the transmitter acting as an interferer in an FDD radio by reducing the dynamic range requirement on the receiver. Additionally, an integrated image reject scheme is used to further reduce spurious image signals.

In accordance with the invention, the first local oscillator (LO) in the image reject receiver is set to coincide with the transmit (TX) band center frequency, or a sub-harmonic of it. In this way, after the first down-conversion is done, the TX interferer is converted to DC, where it can be effectively removed using a simple high-pass filter such as a DC block integrated capacitor. Image rejection is achieved by the use of a two-step down-conversion approach that preferably uses quadrature LOs to implement a single-sideband down-converter.

The above solution provides for a receiver section that can be integrated helping to reduce the overall cost of the radio solution. Compared to conventional heterodyne receivers, off-chip image reject filters are not required by the design of the preferred embodiment. In addition, compared to direct-conversion architectures, the invention reduces the problem of input second-order intercept point (IIP2) and DC offset requirements caused by the larger interferer from the transmitter.

The preferred embodiment shown in FIG. 1 is implemented using a quasi-homodyne architecture with an important difference. The first local oscillator signal (LO_1I and LO_1Q) provided to the first down conversion section including mixers 106 and 108 is set to the transmit frequency band of transmitter section 126. This sets the transmit leakage after the first down-conversion by mixers 106 and 108 to DC which is then filtered off with high pass filters (HPF) 110, 112. The high pass filters 110, 112 can be implemented with very high linearity and low noise, for example, using a simple DC blocking capacitor or cascaded single pole high pass solutions. This effectively removes the largest interferer in the receiver.

In the preferred embodiment, the radio transceiver shown in FIG. 1 is an FDD radio for use with WCDMA systems. It should be noted that FDD is a radio system in which the radio receives and transmits simultaneously. In an exemplary FDD system, the transmitter section power amplifier 128 outputs power at around 25 dbm, which after it makes it through duplexer 102 is about -25 dbm at the low noise amplifier (LNA) 104 input.

These high power signals act as "jammers" to the receiver section and are removed by the High-Pass filters (HPFs) 110 and 112. Image suppression is implemented in the circuit through filtering in the duplexer 102, the tuned LNA 104 and the six image rejection mixers 114, 116, 118, 120, 106 and 108. The second down conversion section of the receiver includes mixers 114, 116, 118 and 120 that help implement a single-sideband down converter.

In a typical example of the present invention, if the transmit frequency of radio 100 is set at 1.96 Gigahertz (GHz) and the receive frequency is at 2.1 GHz then LO_1I and LO_1Q use the transmit frequency of 1.96 GHz (or a sub-harmonic thereof) provided by transmitter section 126 as the LO signal for mixers 106 and 108, which leaves an intermediate frequency (IF) of 200 MHz, which is lowered to baseband by mixers 114, 116, 118 and 120 using LO_2I and LO_2Q. Adder 122 then provides the In-phase base band signal (B.B.I.) 130, while adder 124 provides the Quadrature base band signal (B.B.Q.) 132

Some of the advantages of the present invention include, effectively removing the largest interferer in the receiver by moving the transmit frequency to DC and high-pass filtering it. Secondly, image rejection is achieved on-chip without external SAW filters that require off-chip matching and also introduce in-band losses and increase the cost of the design. Thirdly, since the DC and IIP2 components introduced by the TX interferer are removed after the first mixers 106 and 108, linearity and DC offset constraints are reduced considerably. Finally, since the TX LO is generated in the transmitter, there is no need to generate a separate high frequency LO for the receiver.

While the preferred embodiments of the invention have been illustrated and described, it will be clear that the invention is not so limited. Numerous modifications, changes, variations, substitutions and equivalents will occur to those skilled in the art without departing from the spirit and scope of the present invention as defined by the appended claims.